

OM1412-X EoS HOLO VMAP 10G



Virtual ASSP

10G Gb/s, 192 Group HOLO Ethernet(SPI4.2) over Sonet/SDH Mapper

Description

The OM1412 is an highly integrated, ultra compact **10Gb/s, High and Low Order, Ethernet over Sonet/SDH Packet Mapper** 'Virtual ASSP' targeted to the Xilinx Virtex 5 Family. 10Gb/s of channelized Ethernet is transported over High Order or Low Order Sonet/SDH (EOS) using standards complaint GFP-F, VCAT and LCAS. Up to 25% of the 10G bandwidth can be low order traffic.

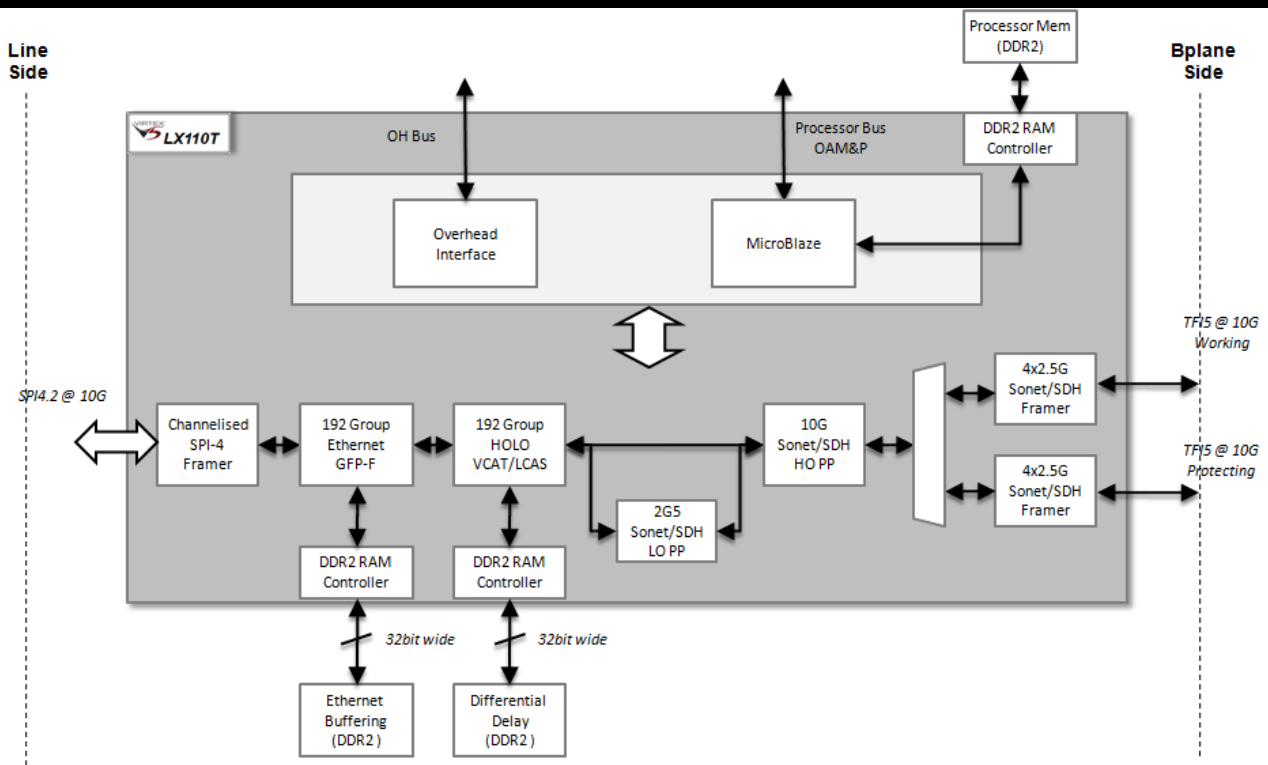
The 'packet' interface is SPI4.2 and supports 192 channels allowing more individual customers to be handled on a single device further reducing opex. The 'Sonet/SDH' interface is 10Gb/s 1+1 protected TF15 interface for high reliability carrier grade deployments.

The OM1412 handles both 'Real Concatenation' (CCAT) and 'Virtual Concatenation' (VCAT). In addition, LCAS is supported to allow group bandwidth to be hitlessly increased or decreased as customer need dictates.

The OM1412 has been designed from the ground up as cost effective ASSP replacement in an FPGA – ultra-compact IP targeting the lowest cost FPGA, highly integrated design with CDR, Framer, Mapper and SPI4.2 interface in a single package, 32bit wide DDR2 for external packet buffer and external differential delay memory (up to 64ms), Software Device Driver and on-chip debugger and supporting toolchain - all lower cost and accelerate TTM.

Typical applications are in Metro Core head end products supporting many EOS VCAT/GFP streams from multiple Access Network customers into a single 10GbE stream for handoff to the Data Core Network.

Block Diagram



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Features

Backplane Interfaces

- 2 x 10G TF15 supporting 1+1 Equipment Protection.

Network Interfaces

- 10G - SPI4.1 622Mhz LVDS for direct connection to NPU or TM.

Sonet/SDH

- Sonet/SDH G.707/T1.105 compliant.
- SDH Mappings - AU4-64c, 16c, 4c, AU4, AU3
- Sonet Mappings – STS1, STS3c, 12c, 48c, 192c SPE
- SDH Payloads – VC11, VC12, VC3, VC4, VC4-4c, 16c, 64c
- Sonet Payloads – VT1.5, VT2, STS1, STS3c, 12c, 48c, 192c
- Full SOH & POH Processing.
- Bandwidth Management of 100% High Order Payload and 25% of Low Order Payload.
- Overhead Insert/Extract over external bus for mate to mate or linecard to switch signalling.

GFP/VCAT/LCAS

- 192 VCAT Groups (10G), individually rate configurable.
- GFP-F (G.7041), Mapping support.
- VCAT Payloads VT1.5, VT2, VC11, VC12, STS1, STS3c, VC3 and VC4.
- 'Any to any' payload to VCAT group assignment.
- 64ms differential delay using external low-cost DDR2 memory.
- LCAS support (ITU G.7042) for hitless dynamic bandwidth adjustment.
- LCAS to non-LCAS interworking.
- Support for Client Management Frames

Ethernet

- SPI4.2 Channelised Interface.
- External packet buffer in low cost DDR2 memory.
- Jumbo Frame support.

OAM

- 16 bit OAM Bus for configuration, performance monitoring, alarm reporting and event reporting.

Benefits

Low Cost.

- Ultra-compact design.
- Single Device Design.
- Low cost DDR2 Memory.

Global Application.

- Sonet T1.105 and SDH G.707 support.

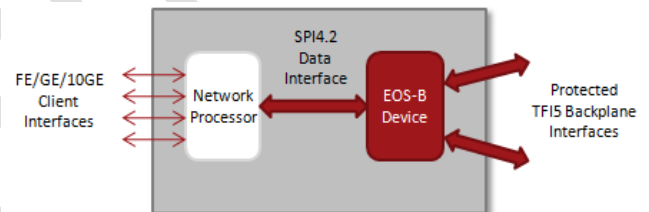
Unparalleled Development and Support Tools.

- OmniSPY and OmniTEST support tools reduce development time and costs by up to 50%.

Adaptable Design

- Interface adaptations incorporated in the device further reduce peripherals and costs

Applications



Target Devices & Customisation

SX95T, LX110T or LX155T depending requirements. FF1136 pin compatible packages.

Typical Customisations :

SPI4.2 adaptation to support NPU vendor extensions.

External Overhead Bus adaption to eliminate external 'glue' logic.

Omiino is happy to consider other customisation requests.

Contacts

For more information please contact sales@omiino.com