

OM1312-X EoS HOLO VMAP 2G5



Virtual ASSP

2.5 Gb/s, 128 Group HOLO Ethernet(SPI3) over Sonet/SDH Mapper

Description

The OM1312 is a highly integrated, ultra compact **2.5Gb/s, High and Low Order, Ethernet over Sonet/SDH Packet Mapper** 'Virtual ASSP' targeted to the Xilinx Virtex 5 Family. 2.5Gb/s of channelized Ethernet is transported over High Order or Low Order Sonet/SDH (EOS) using standards compliant GFP-F, VCAT and LCAS.

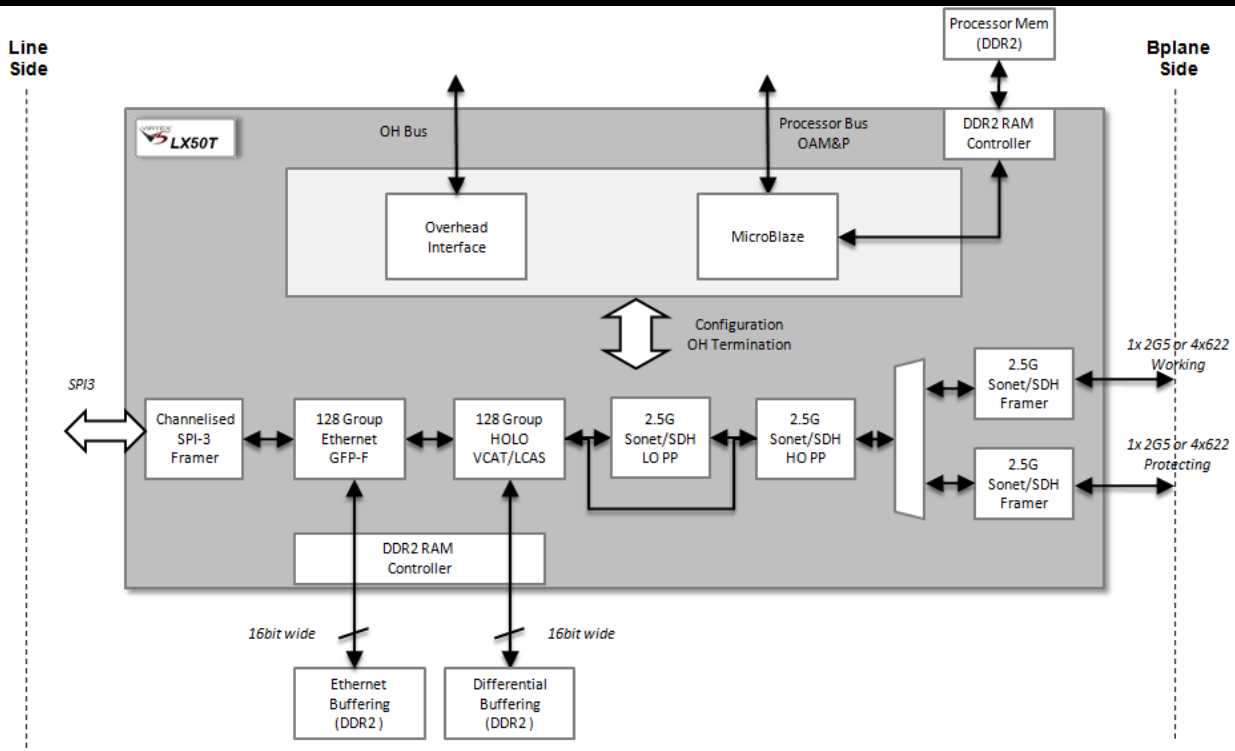
The 'packet' interface is SPI3 and supports 128 channels allowing more individual customers to be handled on a single device further reducing opex. The 'Sonet/SDH' backplane interface is 1+1 protected operating at either 1x2G5 or 4x622M for high reliability carrier grade deployments.

The OM1312 handles both 'Real Concatenation' (CCAT) and 'Virtual Concatenation' (VCAT). In addition, LCAS is supported to allow group bandwidth to be hitlessly increased or decreased as customer need dictates.

The OM1312 has been designed from the ground up as cost effective ASSP replacement in an FPGA – ultra-compact IP targeting the lowest cost FPGA, highly integrated design with CDR, Framer, Mapper and SPI3 interface in a single package, two 16-bit wide DDR2 memories for external packet buffer and external differential delay support (up to 64ms), Software Device Driver and on-chip debugger and supporting toolchain - all features which lower BOM cost and accelerate TTM.

Typical applications are in Metro Core head end products supporting many EOS VCAT/GFP streams from multiple Access Network customers into a single 2.5GbE stream for handoff to the Data Core Network.

Block Diagram



OM1312-X EoS HOLO VMAP 2G5



Virtual ASSP

2.5 Gb/s, 128 Group HOLO Ethernet(SPI3) over Sonet/SDH Mapper

Features

Backplane Interfaces

- Protected 2G5 for 1+1 Equipment Protection
- OR Protected 4x622 for 1+1 Equipment Protection.

Network Interfaces

- 2G5 – SPI3 for direct connection to NPU or TM.

Sonet/SDH

- Sonet/SDH G.707/T1.105 compliant.
- SDH Mappings – AU4- 16c, 4c, AU4, AU3
- Sonet Mappings – STS1, STS3c, 12c, 48c SPE
- SDH Payloads – VC11, VC12, VC3, VC4, VC4-4c, 16c
- Sonet Payloads – VT1.5, VT2, STS1, STS3c, 12c, 48c.
- Full SOH & POH Processing.
- Overhead Insert/Extract over external bus for mate to mate or linecard to switch signalling.

GFP/VCAT/LCAS

- 128 VCAT Groups individually rate configurable.
- GFP-F (G.7041), Mapping support.
- VCAT Payloads VT1.5, VT2, VC11, VC12, STS1, STS-3c, VC3 and VC4.
- 'Any to any' payload to VCAT group assignment.
- 64ms differential delay using external low-cost DDR2 memory.
- LCAS support (ITU G.7042) for hitless dynamic bandwidth adjustment.
- LCAS to non-LCAS interworking.
- Support for Client Management Frames

Ethernet

- SPI3 Channelised Interface.
- External packet buffer in low cost DDR2 memory.

OAM

- 16 bit OAM Bus for configuration, performance monitoring, alarm reporting and event reporting.

Benefits

Low Cost.

- Ultra-compact design.
- Single Device Design.
- Low cost DDR2 Memory.

Global Application.

- Sonet T1.105 and SDH G.707 support.

Unparalleled Development and Support Tools.

- OmniSPY and OmniTEST support tools reduce development time and costs by up to 50%.

Adaptable Design

- Interface adaptations incorporated in the device further reduce peripherals and costs

Applications

- MSPP EoS Headend Linecards.
- DWDM Ethernet Sub-Rate Linecards/Muxponders.
- Hybrid Data/Sonet Fabric Interconnect Blind Linecards.

Target Devices & Customisation

LX50T to LX85T depending features. FF1136 pin compatible packages.

Typical Customisations :

SPI3 adaptation to support NPU vendor extensions.

External Overhead Bus adaption to eliminate external 'glue' logic.

Omiino is happy to consider other customisation requests.

Contacts

For more information please contact info@omiino.com